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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,373	01/14/2004	Kazumi Hara	9319I-000647	3618

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,373	HARA, KAZUMI	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) *1-4,9-18,23-33,35-41 and 43-70* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8,19-22,34 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/757373 Attorney's Docket #: 93191-000647
Filing Date: 1/14/2004; claimed foreign priority to 1/15/2003

Applicant: Hara et al.

Examiner: Alexander Williams

Applicant's election with traverse of species I (claims 5-8, 19-22, 34 and 42), filed 11/22/05, has been acknowledged.

This application contains claims 1-4, 9-18, 23-33, 35-41 and 43-70 drawn to an invention non-elected with traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: Related information should be updated.

Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on an insulating layer, a first section of the insulating layer and a second portion of the insulating layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece]

structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 5-8, 19-22, 34 and 42 are rejected under 35 U.S.C. § 103(a) as being unpatentable over in view of Taniguchi et al. (U.S. Patent # 6,768,205 B2).

5. Taniguchi et al. (figures 1 to 11) specifically figure 4 show a semiconductor chip **20** comprising:

a semiconductor substrate **21**;

an integrated circuit, at least a part of the integrated circuit being formed in the semiconductor substrate;

a penetrating electrode **21D,21E** which is formed through the semiconductor substrate from

a first surface to a second surface of the semiconductor substrate and has a projection which projects from the second surface;

an insulating layer **22,21C** formed over an entire surface of the second surface,

wherein the insulating layer includes a first insulating section **(inner portion of 22,lower portion of 21C)** formed in a region

around the projection and a second insulating section **(outer portion of 22)** other than the first insulating section, and

wherein the second insulating section **(outer portion of 22)** is formed to be thinner than a thickest area of the first insulating section.

6. The semiconductor chip as defined in claim 5, Taniguchi et al. show wherein the first insulating section is formed so that a thickness of the first insulating section decreases as a distance from the projection increases.

7. The semiconductor chip as defined in claim 5, Taniguchi et al. show wherein the projection is formed 15 to have a height higher than a height of a thickest area of the insulating layer.

8. The semiconductor chip as defined in claim 5, Taniguchi et al. show wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

19. Taniguchi et al. (figures 1 to 11) specifically figure 4 show a semiconductor wafer **20** comprising:

a semiconductor substrate **21**;

a plurality of integrated circuits, at least a part of each of the integrated circuits being formed in the semiconductor substrate;

a plurality of penetrating electrodes **21D**, each of the penetrating electrodes being formed through the semiconductor substrate from a first surface to a second surface of the semiconductor substrate and having a projection which projects from the second surface;

an insulating layer **22,21C** formed over an entire surface of the second surface, wherein the insulating layer includes a plurality of first insulating sections **(inner portion of 22,lower portion of 21C)** and a second insulating section **(outer portion of 22)** other than the first insulating sections, each of the first insulating sections being formed in a region around the projection, and

wherein the second insulating section is formed to be thinner than a thickest area of each of the first insulating sections.

20. The semiconductor wafer as defined in claim 19, Taniguchi et al. show wherein each of the first insulating sections is formed so that a thickness of each of the first insulating sections decreases as a distance from the projection increases.

21. The semiconductor wafer as defined in claim 19, Taniguchi et al. show wherein the projection is formed to have a height higher than a height of a thickest area of the insulating layer.

22. The semiconductor wafer as defined in claim 19, Taniguchi et al. show wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

42. Taniguchi et al. show an electronic instrument comprising the semiconductor chip as defined in claim 5.

Therefore, it would have been obvious to one of ordinary skill in the art to use the insulating layer, first section of the insulating layer and the section section of the insulating layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

(34) Further, the present invention solves the above problems by providing a via formed substrate, and a forming method thereof, as follows. The via formed substrate includes a supporting substrate having a first principal plane and a second principal plane that counters the first principal plane, through holes in a first diameter extending from the second principal plane toward the first principal plane of the supporting substrate, tapered sections formed to the through holes at an end section toward the first principal plane with openings of a second diameter that is larger than the first diameter at the first principal plane, conductive plugs that fill up the through holes, and electrode pads that are formed on the tapered sections and are electrically connected to the conductive plugs in a tapered shape corresponding to the tapered sections. The forming method of the via formed substrate described above includes a step of forming tapered concavities on the first

principal plane of the semiconductor substrate by anisotropic etching, a step of forming an insulation layer in a shape corresponding to the tapered concavities and covering the surface of the tapered concavities, a step of forming the via holes that extend from the second principal plane that counters the first principal plane to the first principal plane such that the via holes expose the insulation layer at the tapered concavity section, a step of forming the electrode pads on the insulation layer in a shape corresponding to the top shape of the tapered section such that the tapered sections are surrounded, and a step of forming the via plugs by filling up the via holes with conductive materials.

(9) With regard to the structure of FIG. 3(E), the etching stop film 22 extends from the bottom end of the through holes 21A corresponding to the bottom principal plane of the Si substrate 21 toward the center of the through holes in a distance corresponding to the thickness of the side wall oxide-film 21C. The edge of the side wall oxide-film 21C touches the upper surface of the etching stop film 22.

(11) FIG. 4 shows a structure of the thin-film circuit substrate 20 formed as above, wherein via plugs are formed, and solder vamps are further formed.

(12) With reference to FIG. 4, via plugs 21D made of a low resistance metal, such as Cu and W, are formed in the through holes 21A, filling up the through holes 21A, and electrode pads 21E made of Pt or Au are formed at the upper edge of the via plugs 21D.

(13) On the bottom side, corresponding to the via plugs 21D, electrode pads 21F are formed on the thin film circuit 24, and vamp electrodes of a solder ball 25 are formed on the electrode pads 21F.

(14) In the thin-film circuit substrate 20 with the structure of FIG. 4, the thin-film circuit 24 is formed before forming the via plugs 21D. A heat treatment in a high temperature oxidization atmosphere is not necessary after forming the via plugs 21D. In this manner, the problem of destruction of the thin film circuit 24 due to an expansion of the via plugs 21D by oxidization does not arise.

(15) As above, in the thin-film circuit substrate 20 structured as shown in FIG. 4, a process for removing existing electrode pads by polishing, which is required in the case that a ceramic substrate of FIG. 1(A) and FIG. 1(B) is used, is made unnecessary by using Si substrate. Further, it is possible to form through holes 21A, therefore via plugs 21D, of a highly minute diameter with a very fine repetition pitch.

(16) FIG. 5(A), FIG. 5(B), FIG. 5(C), FIG. 6(D), FIG. 6(E), and FIG. 6(F) show a manufacturing method of a thin-film circuit substrate 20A by the second embodiment of the present invention. Here, regarding a portion explained previously, the same reference numbers are given in the figures and an explanation is omitted.

(17) With reference to FIG. 5(A), a SiN pattern 31 that will become an etching stop film is formed on the bottom principal plane of the Si substrate 21 corresponding to via holes to be formed. In the process of FIG. 5(B), a thermal oxidation processing is performed on the Si substrate 21 of FIG. 5(A). Consequently, as shown in FIG. 5(B), a thermal oxidation film 32 is formed in a self-alignment manner on the both sides of the SiN pattern 31 of the bottom principal plane of the Si substrate 21.

(18) Next, in the process of FIG. 5(C), a resist film 23 which has resist opening 23A corresponding to the via holes to be formed on the top principal plane of the Si substrate 21 is formed like the process of FIG. 3(B). In the process of FIG. 6(D), dry etching of the Si substrate 21 is carried out until the SiN etching stop pattern 31 is exposed, using the resist film 23 as a mask such that the through hole 21A is formed in the Si substrate 21 corresponding to the resist opening 23A. In the above dry etching process for forming the through holes 21A, etching time is extended such that the so-called over-etching is performed in order that the SiN etching stop pattern 31 is surely exposed in all the through holes 21A of the Si substrate 21, similarly to the previous embodiment.

(19) Further, the resist film 23 is removed in the process of FIG. 6(E), and an insulator layer 21C is formed by a thermal oxidation process or a CVD process on the inner wall surface of the through holes 21A formed by the process of FIG. 6(D). Moreover, in the process of FIG. 6(E), the thin-film

circuit 24 is formed on the thermal oxidation film 32 on the bottom principal plane of the Si substrate 21. The thin-film circuit 24 may include a ferroelectric film or a high dielectric film, as explained previously, and in that case, a heat treatment in an oxidization atmosphere is performed for crystallization and oxygen deficit compensation.

(20) Further, in the process of FIG. 6(F), the SiN etching pattern 31 is removed by a selective etching process, and the thin-film circuit is exposed.

(21) After the process of FIG. 6(F), the thin-film circuit substrate 20A that is almost the same as FIG. 4 is obtained by filling the via holes 21A with a metal such as Cu and W.

(22) In this embodiment, the thermal oxidation film 32 is formed, in the self-alignment manner, on the both sides of the SiN etching stop pattern 31 on the bottom principal plane of the Si substrate 21 in the process of FIG. 5(B). For this reason, there is an advantage in that the insulation layer of the side wall is secured, and opening is surely achieved by the selective etching of FIG. 6(F).

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/773,774,700-703,758,751,778,734, 737,738,777, 685, 686,680,678,687,696,698,690-693	1/31/05
Other Documentation: foreign patents and literature in 257/773,774,700-703,758,751,778,734, 737,738,777, 685, 686,680,678,687,696,698,690-693	1/31/05
Electronic data base(s): U.S. Patents EAST	1/31/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/31/06